CS5159

CPU 5-Bit Synchronous Buck Controller

The CS5159 is a 5−bit synchronous dual N−Channel buck controller. It is designed to provide unprecedented transient response for today's demanding high−density, high−speed logic. The regulator operates using a proprietary control method, which allows a 100 ns response time to load transients. The CS5159 is designed to operate over a 4.25−16 V range (V_{CC}) using 12 V to power the IC and 5.0 V or 12V as the main supply for conversion.

The CS5159 is specifically designed to power Pentium® II processors and other high performance core logic. It includes the following features: on board, 5−bit DAC, short circuit protection, 1.0% output tolerance, V_{CC} monitor, and programmable Soft Start capability. The CS5159 is available in 16 pin surface mount.

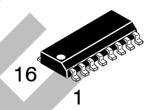
Features

- Dual N−Channel Design
- Excess of 1.0 MHz Operation
- 100 ns Transient Response
- 5−Bit DAC
- Backward Compatible with Adjustable CS5157
- 30 ns Gate Rise/Fall Times
- 1.0% DAC Accuracy
- 5.0 V & 12 V Operation
- Remote Sense
- Programmable Soft Start
- Lossless Short Circuit Protection
- V_{CC} Monitor
- 25 ns FET Nonoverlap Time
- V^2™ Control Topology
- Current Sharing
- Overvoltage Protection

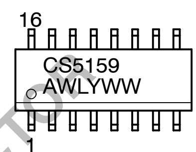
ON Semiconductor™

http://onsemi.com

MARKING DIAGRAM

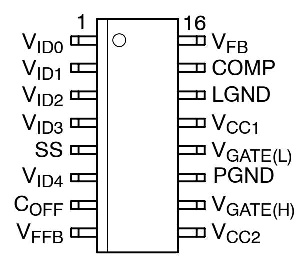


SOIC−16
D SUFFIX
CASE 751B



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping
CS5159GD16	SO−16	48 Units/Rail
CS5159GDR16	SO−16	2500 Tape & Reel

July, 2006 − Rev. 5

Publication Order Number:
CS5159/D

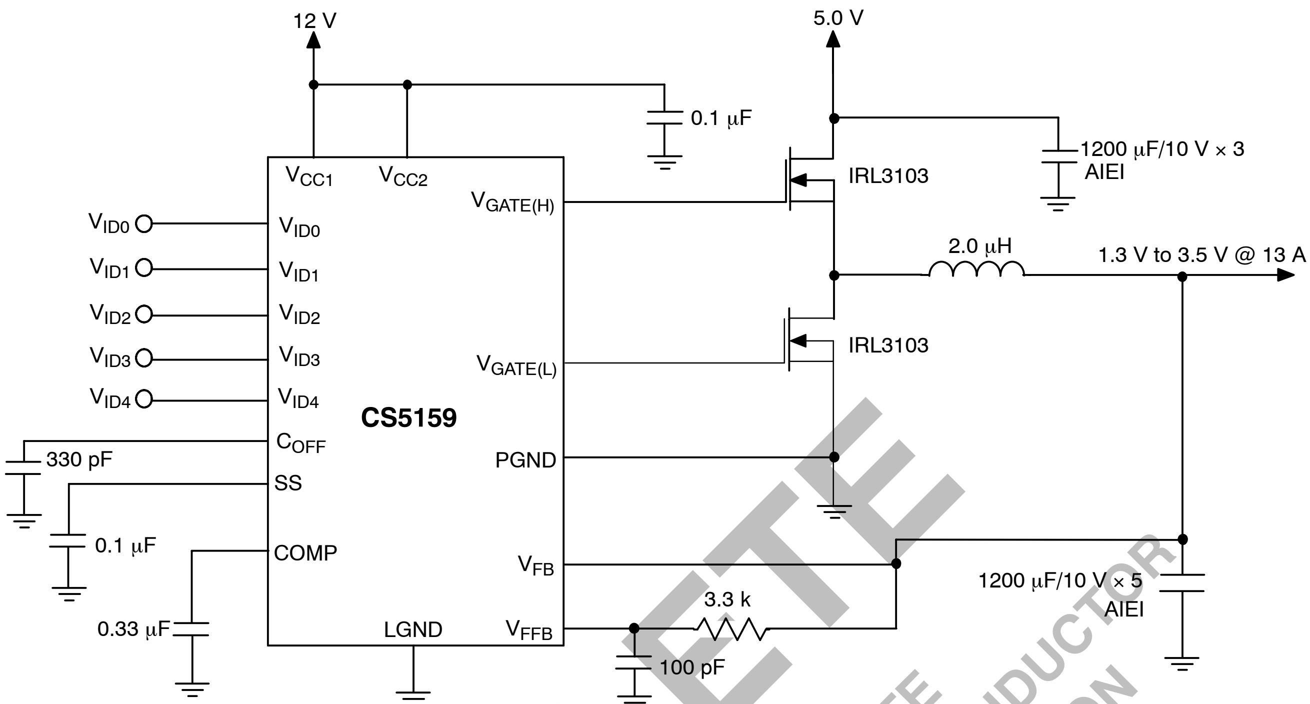


Figure 1. Application Diagram, Switching Power Supply for Core Logic – Pentium® II Processor

ABSOLUTE MAXIMUM RATINGS*

Rating		Value	Unit
Operating Junction Temperature, T_J		0 to 150	°C
Lead Temperature Soldering:	Reflow: (SMD styles only) (Note 1)	230 peak	°C
Storage Temperature Range, T_S		−65 to +150	°C
ESD Susceptibility (Human Body Model)		2.0	kV

1. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

ABSOLUTE MAXIMUM RATINGS

Pin Name	Max Operating Voltage	Max Current
V_{CC1}	16 V/−0.3 V	25 mA DC/1.5 A peak
V_{CC2}	18 V/−0.3 V	20 mA DC/1.5 A peak
SS	6.0 V/−0.3 V	−100 μA
COMP	6.0 V/−0.3 V	200 μA
V_{FB}	6.0 V/−0.3 V	−0.2 μA
C_{OFF}	6.0 V/−0.3 V	−0.2 μA
V_{FFB}	6.0 V/−0.3 V	−0.2 μA
V_{ID0} – V_{ID4}	6.0 V/−0.3 V	−50 μA
$V_{GATE(H)}$	18 V/−0.3 V	100 mA DC/1.5 A peak
$V_{GATE(L)}$	16 V/−0.3 V	100 mA DC/1.5 A peak
LGND	0 V	25 mA
PGND	0 V	100 mA DC/1.5 A peak

ELECTRICAL CHARACTERISTICS ($0°C < T_A < +70°C$; $0°C < T_J < +85°C$; $8.0 V < V_{CC1} < 14 V$; $5.0 V < V_{CC2} < 18 V$; DAC Code: $V_{ID4} = V_{ID2} = V_{ID1} = V_{ID0} = 1$; $V_{ID3} = 0$; $CV_{GATE(L)}$ and $CV_{GATE(H)} = 1.0 nF$; $C_{OFF} = 330 pF$; $C_{SS} = 0.1 \mu F$, unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Error Amplifier					
V_{FB} Bias Current	$V_{FB} = 0 V$	–	0.3	1.0	μA
Open Loop Gain	$1.25 V < V_{COMP} < 4.0 V$; Note 2	50	60	–	dB
Unity Gain Bandwidth	Note 2	500	3000	–	kHz
COMP SINK Current	$V_{COMP} = 1.5 V$; $V_{FB} = 3.0 V$; $V_{SS} > 2.0 V$	0.4	2.5	8.0	mA
COMP SOURCE Current	$V_{COMP} = 1.2 V$; $V_{FB} = 2.7 V$; $V_{SS} = 5.0 V$	30	50	80	μA
COMP CLAMP Current	$V_{COMP} = 0 V$; $V_{FB} = 2.7 V$	0.4	1.0	1.6	mA
COMP High Voltage	$V_{FB} = 2.7 V$; $V_{SS} = 5.0 V$	4.0	4.3	5.0	V
COMP Low Voltage	$V_{FB} = 3.0 V$	–	160	600	mV
PSRR	$8.0 V < V_{CC1} < 14 V$ @ 1.0 kHz; Note 2	60	85	–	dB
V_{CC1} Monitor					
Start Threshold	Output switching	3.75	3.90	4.05	V
Stop Threshold	Output not switching	3.70	3.85	4.00	V
Hysteresis	Start−Stop	–	50	–	mV
$V_{GATE(H)}$ and $V_{GATE(L)}$					
Out SOURCE Sat at 100 mA	Measure $V_{CC1} - V_{GATE(L)}$; $V_{CC2} - V_{GATE(H)}$	–	1.2	2.0	V
Out SINK Sat at 100 mA	Measure $V_{GATE(H)} - V_{PGND}$; $V_{GATE(L)} - V_{PGND}$	–	1.0	1.5	V
Out Rise Time	$1.0 V < V_{GATE(H)} < 9.0 V$; $1.0 V < V_{GATE(L)} < 9.0 V$; $V_{CC1} = V_{CC2} = 12 V$	–	30	50	ns
Out Fall Time	$9.0 V > V_{GATE(H)} > 1.0 V$; $9.0 V > V_{GATE(L)} > 1.0 V$; $V_{CC1} = V_{CC2} = 12 V$	–	30	50	ns
Delay $V_{GATE(H)}$ to $V_{GATE(L)}$	$V_{GATE(H)}$ falling to 2.0 V; $V_{CC1} = V_{CC2} = 8.0 V$; $V_{GATE(L)}$ rising to 2.0 V	–	25	50	ns
Delay $V_{GATE(L)}$ to $V_{GATE(H)}$	$V_{GATE(L)}$ falling to 2.0 V; $V_{CC1} = V_{CC2} = 8.0 V$; $V_{GATE(H)}$ rising to 2.0 V	–	25	50	ns
$V_{GATE(H)}$, $V_{GATE(L)}$ Resistance	Resistor to LGND, Note 2	20	50	100	kΩ
$V_{GATE(H)}$, $V_{GATE(L)}$ Schottky	LGND to $V_{GATE(H)}$ @ 10 mA LGND to $V_{GATE(L)}$ @ 10 mA	–	600	800	mV
Soft Start (SS)					
Charge Time	–	1.6	3.3	5.0	ms
Pulse Period	–	25	100	200	ms
Duty Cycle	(Charge Time /Pulse Period) × 100	1.0	3.3	6.0	%
COMP Clamp Voltage	$V_{FB} = 0 V$; $V_{SS} = 0$	0.50	0.95	1.10	V
V_{FFB} SS Fault Disable	$V_{GATE(H)}$ = Low; $V_{GATE(L)}$ = Low	0.9	1.0	1.1	V
High Threshold	–	–	2.5	3.0	V
PWM Comparator					
Transient Response	V_{FFB} = 0 to 5.0 V to $V_{GATE(H)}$ = 9.0 V to 1.0 V; $V_{CC1} = V_{CC2} = 12 V$	–	100	125	ns
V_{FFB} Bias Current	$V_{FFB} = 0 V$	–	0.3	–	μA

2. Guaranteed by design, not 100% tested in production.

ELECTRICAL CHARACTERISTICS (continued) (0°C < T_A < +70°C; 0°C < T_J < +85°C; 8.0 V < V_{CC1} < 14 V; 5.0 V < V_{CC2} < 18 V; DAC Code: $V_{ID4} = V_{ID2} = V_{ID1} = V_{ID0} = 1$; $V_{ID3} = 0$; $CV_{GATE(L)}$ and $CV_{GATE(H)}$ = 1.0 nF; C_{OFF} = 330 pF; C_{SS} = 0.1 μF, unless otherwise specified.)

Characteristic					Test Conditions	Min	Typ	Max	Unit
DAC									
Input Threshold					V_{ID0}, V_{ID1}, V_{ID2}, V_{ID3}, V_{ID4}	1.00	1.25	2.40	V
Input Pull Up Resistance					V_{ID0}, V_{ID1}, V_{ID2}, V_{ID3}, V_{ID4}	25	50	100	kΩ
Pull Up Voltage					–	4.85	5.00	5.15	V
Accuracy (all codes except 11111, 10110, 10101, 10100, 10011, 10010, 10001, 10000)					Measure $V_{FB} = V_{COMP}$, $25°C \le T_J \le 85°C$	–	–	1.0	%
V_{ID4}	V_{ID3}	V_{ID2}	V_{ID1}	V_{ID0}					
0	1	1	1	1	–	1.2870	1.3000	1.3130	V
0	1	1	1	0	–	1.3365	1.3500	1.3635	V
0	1	1	0	1	–	1.3860	1.4000	1.4140	V
0	1	1	0	0	–	1.4355	1.4500	1.4645	V
0	1	0	1	1	–	1.4850	1.5000	1.5150	V
0	1	0	1	0	–	1.5345	1.5500	1.5655	V
0	1	0	0	1	–	1.5840	1.6000	1.6160	V
0	1	0	0	0	–	1.6335	1.6500	1.6665	V
0	0	1	1	1	–	1.6830	1.7000	1.7170	V
0	0	1	1	0	–	1.7325	1.7500	1.7675	V
0	0	1	0	1	–	1.7820	1.8000	1.8180	V
0	0	1	0	0	–	1.8315	1.8500	1.8685	V
0	0	0	1	1	–	1.8810	1.9000	1.9190	V
0	0	0	1	0	–	1.9305	1.9500	1.9695	V
0	0	0	0	1	–	1.9800	2.0000	2.0200	V
0	0	0	0	0	–	2.0295	2.0500	2.0705	V
1	1	1	1	1	–	1.2191	1.2440	1.2689	V
1	1	1	1	0	–	2.0790	2.1000	2.1210	V
1	1	1	0	1	–	2.1780	2.2000	2.2220	V
1	1	1	0	0	–	2.2770	2.3000	2.3230	V
1	1	0	1	1	–	2.3760	2.4000	2.4240	V
1	1	0	1	0	–	2.4750	2.5000	2.5250	V
1	1	0	0	1	–	2.5740	2.6000	2.6260	V
1	1	0	0	0	–	2.6730	2.7000	2.7270	V
1	0	1	1	1	–	2.7720	2.8000	2.8280	V
1	0	1	1	0	–	2.8420	2.9000	2.9580	V
1	0	1	0	1	–	2.9400	3.0000	3.0600	V
1	0	1	0	0	–	3.0380	3.1000	3.1620	V
1	0	0	1	1	–	3.1360	3.2000	3.2640	V
1	0	0	1	0	–	3.2340	3.3000	3.3660	V
1	0	0	0	1	–	3.3320	3.4000	3.4680	V
1	0	0	0	0	–	3.4300	3.5000	3.5700	V

ELECTRICAL CHARACTERISTICS (continued) (0°C < T_A < +70°C; 0°C < T_J < +85°C; 8.0 V < V_{CC1} < 14 V; 5.0 V < V_{CC2} < 18 V; DAC Code: V_{ID4} = V_{ID2} = V_{ID1} = V_{ID0} = 1; V_{ID3} = 0; $CV_{GATE(L)}$ and $CV_{GATE(H)}$ = 1.0 nF; C_{OFF} = 330 pF; C_{SS} = 0.1 μF, unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Supply Current					
I_{CC1}	No Switching	–	8.5	13.5	mA
I_{CC2}	No Switching	–	1.6	3.0	mA
Operating I_{CC1}	V_{FB} = COMP = V_{FFB}	–	8.0	13	mA
Operating I_{CC2}	V_{FB} = COMP = V_{FFB}	–	2.0	5.0	mA
C_{OFF}					
Normal Charge Time	V_{FFB} = 1.5 V; V_{SS} = 5.0 V	1.0	1.6	2.2	μs
Extension Charge Time	V_{SS} = V_{FFB} = 0	5.0	8.0	11.0	μs
Discharge Current	C_{OFF} to 5.0 V; V_{FB} > 1.0 V	5.0	–	–	mA
Time Out Timer					
Time Out Time	V_{FB} = V_{COMP}; V_{FFB} = 2.0 V; Record $V_{GATE(H)}$ Pulse High Duration	10	30	65	μs
Fault Mode Duty Cycle	V_{FFB} = 0V	35	50	70	%

PACKAGE PIN DESCRIPTION

PACKAGE PIN # SO–16	PIN SYMBOL	FUNCTION
1, 2, 3, 4, 6	V_{ID0}–V_{ID4}	Voltage ID DAC input pins. These pins are internally pulled up to 5.0 V providing logic ones if left open. V_{ID4} selects the DAC range. When V_{ID4} is High (logic one), the DAC range is 2.10 V to 3.50 V with 100 mV increments. When V_{ID4} is Low (logic zero), the DAC range is 1.30 V to 2.05 V with 50 mV increments. V_{ID0} – V_{ID4} select the desired DAC output voltage. Leaving all 5 DAC input pins open results in a DAC output voltage of 1.2440 V, allowing for adjustable output voltage, using a traditional resistor divider.
5	SS	Soft Start Pin. A capacitor from this pin to LGND in conjunction with internal 60 μA current source provides Soft Start function for the controller. This pin disables fault detect function during Soft Start. When a fault is detected, the Soft Start capacitor is slowly discharged by internal 2.0 μA current source setting the time out before trying to restart the IC. Charge/discharge current ratio of 30 sets the duty cycle for the IC when the regulator output is shorted.
7	C_{OFF}	A capacitor from this pin to ground sets the time duration for the on board one shot, which is used for the constant off time architecture.
8	V_{FFB}	Fast feedback connection to the PWM comparator. This pin is connected to the regulator output. The inner feedback loop terminates on time.
9	V_{CC2}	Boosted power for the high side gate driver.
10	$V_{GATE(H)}$	High FET driver pin capable of 1.5 A peak switching current. Internal circuit prevents $V_{GATE(H)}$ and $V_{GATE(L)}$ from being in high state simultaneously.
11	PGND	High current ground for the IC. The MOSFET driver is referenced to this pin. Input capacitor ground and the source of lower FET should be tied to this pin.
12	$V_{GATE(L)}$	Low FET driver pin capable of 1.5 A peak switching current.
13	V_{CC1}	Input power for the IC and low side gate driver.
14	LGND	Signal ground for the IC. All control circuits are referenced to this pin.
15	COMP	Error amplifier compensation pin. A capacitor to ground should be provided externally to compensate the amplifier.
16	V_{FB}	Error amplifier DC feedback input. This is the master voltage feedback which sets the output voltage. This pin can be connected directly to the output or a remote sense trace.

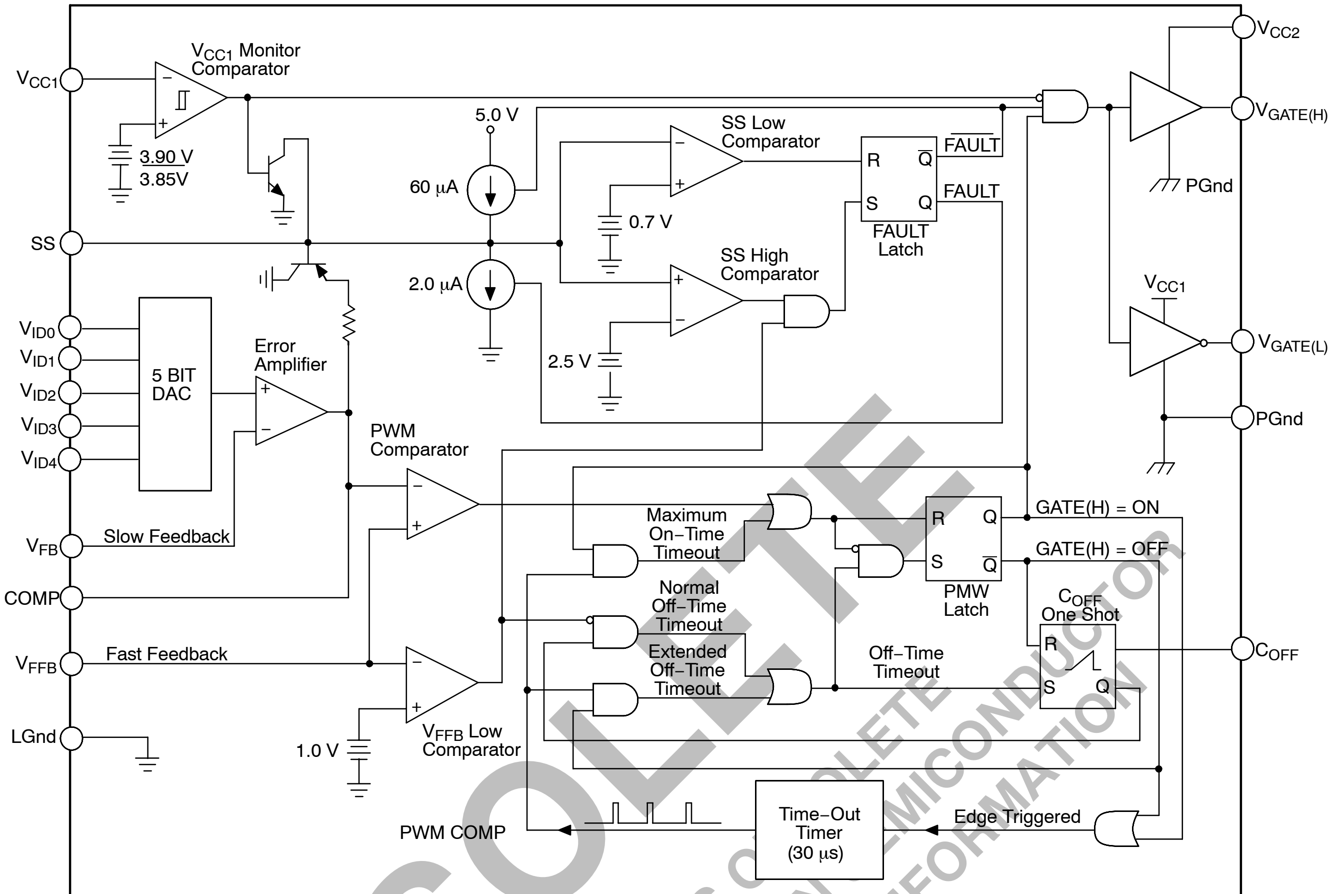


Figure 2. Block Diagram

APPLICATIONS INFORMATION

THEORY OF OPERATION

V^2 Control Method

The V^2 method of control uses a ramp signal that is generated by the ESR of the output capacitors. This ramp is proportional to the AC current through the main inductor and is offset by the value of the DC output voltage. This control scheme inherently compensates for variation in either line or load conditions, since the ramp signal is generated from the output voltage itself. This control scheme differs from traditional techniques such as voltage mode, which generates an artificial ramp, and current mode, which generates a ramp from inductor current.

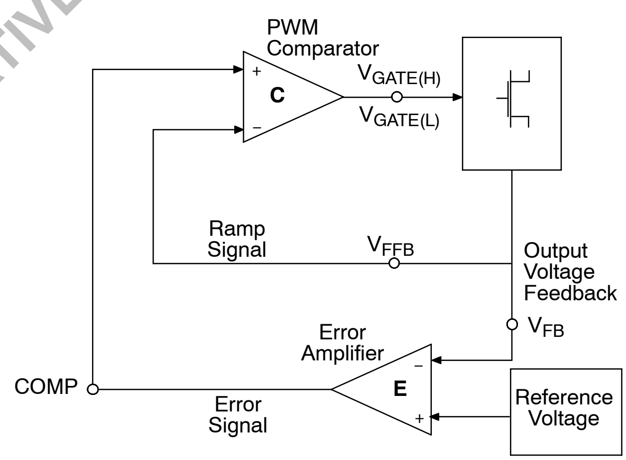


Figure 3. V^2 Control Diagram

The V^2 control method is illustrated in Figure 3. The output voltage is used to generate both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, which allows the control circuit to drive the main switch to 0% or 100% duty cycle as required.

A change in line voltage changes the current ramp in the inductor, affecting the ramp signal, which causes the V^2 control scheme to compensate the duty cycle. Since the change in inductor current modifies the ramp signal, as in current mode control, the V^2 control scheme has the same advantages in line transient response.

A change in load current will have an affect on the output voltage, altering the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. Load transient response is determined only by the comparator response time and the transition speed of the main switch. The reaction time to an output load step has no relation to the crossover frequency of the error signal loop, as in traditional control methods.

The error signal loop can have a low crossover frequency, since transient response is handled by the ramp signal loop. The main purpose of this ‘slow’ feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves remote sensing of the output voltage, since the noise associated with long feedback traces can be effectively filtered.

Line and load regulation are drastically improved because there are two independent voltage loops. A voltage mode controller relies on a change in the error signal to compensate for a deviation in either line or load voltage. This change in the error signal causes the output voltage to change corresponding to the gain of the error amplifier, which is normally specified as line and load regulation. A current mode controller maintains fixed error signal under deviation in the line voltage, since the slope of the ramp signal changes, but still relies on a change in the error signal for a deviation in load. The V^2 method of control maintains a fixed error signal for both line and load variation, since the ramp signal is affected by both line and load.

Constant Off Time

To maximize transient response, the CS5159 uses a constant off time method to control the rate of output pulses. During normal operation, the off time of the high side switch is terminated after a fixed period, set by the C_{OFF} capacitor. To maintain regulation, the V^2 control loop varies switch on time. The PWM comparator monitors the output voltage ramp, and terminates the switch on time.

Constant off time provides a number of advantages. Switch duty cycle can be adjusted from 0 to 100% on a pulse by pulse basis when responding to transient conditions. Both 0% and 100% duty cycle operation can be maintained for extended periods of time in response to load or line transients. PWM slope compensation to avoid sub−harmonic oscillations at high duty cycles is avoided.

Switch on time is limited by an internal 25 μs timer, minimizing stress to the power components.

Programmable Output

The CS5159 is designed to provide two methods for programming the output voltage of the power supply. A five bit on board digital to analog converter (DAC) is used to program the output voltage within two different ranges. The first range is 2.10 V to 3.50 V in 100 mV steps, the second is 1.30 V to 2.05 V in 50 mV steps, depending on the digital input code. If all five bits are left open, the CS5159 enters adjust mode. In adjust mode, the designer can choose any output voltage by using resistor divider feedback to the V_{FB} and V_{FFB} pins, as in traditional controllers.

Start Up

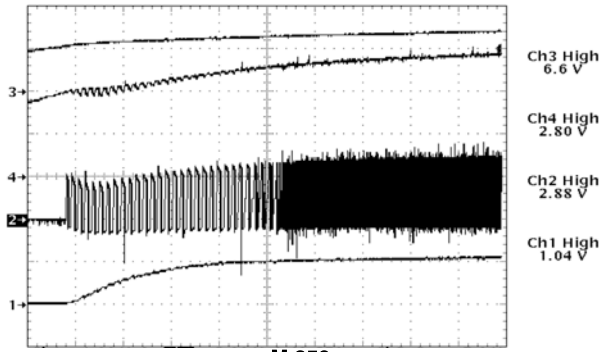
Until the voltage on the V_{CC1} supply pin exceeds the 3.9 V monitor threshold, the Soft Start and gate pins are held low. The FAULT latch is reset (no Fault condition). The output of the error amplifier (COMP) is pulled up to 1.0 V by the comparator clamp. When the V_{CC1} pin exceeds the monitor threshold, the GATE(H) output is activated, and the Soft Start capacitor begins charging. The GATE(H) output will remain on, enabling the NFET switch, until terminated by either the PWM comparator, or the maximum on time timer.

If the maximum on time is exceeded before the regulator output voltage achieves the 1.0 V level, the pulse is terminated. The GATE(H) pin drives low, and the GATE(L) pin drives high for the duration of the extended off time. This time is set by the time out timer and is approximately equal to the maximum on time, resulting in a 50% duty cycle. The GATE(L) pin will then drive low, the GATE(H) pin will drive high, and the cycle repeats.

When regulator output voltage achieves the 1.0 V level present at the COMP pin, regulation has been achieved and normal off time will ensue. The PWM comparator terminates the switch on time, with off time set by the C_{OFF} capacitor. The V^2 control loop will adjust switch duty cycle as required to ensure the regulator output voltage tracks the output of the error amplifier.

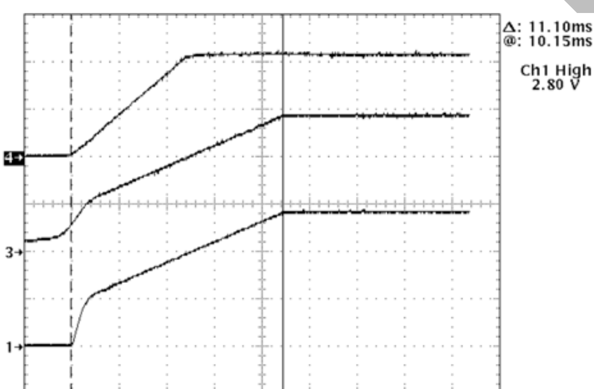
The Soft Start and COMP capacitors will charge to their final levels, providing a controlled turn on of the regulator output. Regulator turn on time is determined by the COMP capacitor charging to its final value. Its voltage is limited by

the Soft Start COMP clamp and the voltage on the Soft Start pin (see Figures 4 and 5).



Trace 1− Regulator Output Voltage (1.0 V/div.)
Trace 2− Inductor Switching Node (2.0 V/div.)
Trace 3− 12 V Input (V_{CC1} and V_{CC2}) (5.0 V/div.)
Trace 4− 5.0 V Input (1.0 V/div.)

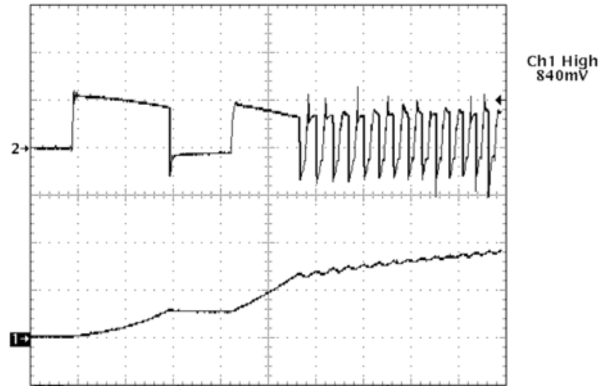
Figure 4. CS5159 Demonstration Board Startup in Response to Increasing 12 V and 5.0 V Input Voltages. Extended Off Time is Followed by Normal Off Time Operation when Output Voltage Achieves Regulation to the Error Amplifier Output.



Trace 1− Regulator Output Voltage (1.0 V/div.)
Trace 3− COMP PIn (error amplifier output) (1.0 V/div.)
Trace 4− Soft Start Pin (2.0 V/div.)

Figure 5. CS5159 Demonstration Board Startup Waveforms

If the input voltage rises quickly, or the regulator output is enabled externally, output voltage will increase to the level set by the error amplifier output more rapidly, usually within a couple of cycles (see Figure 6).

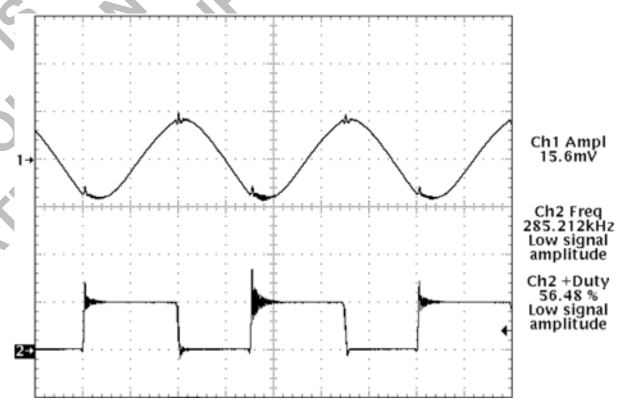


Trace 1− Regulator Output Voltage (5.0 V/div.)
Trace 2− Inductor Switching Node (5.0 V/div.)

Figure 6. CS5159 Demonstration Board Enable Startup Waveforms

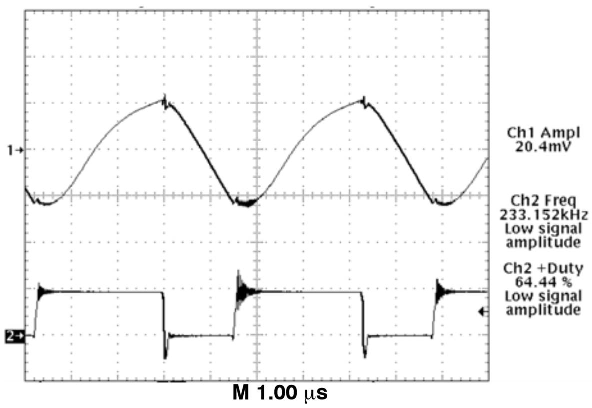
Normal Operation

During normal operation, switch off time is constant and set by the C_{OFF} capacitor. Switch on time is adjusted by the V^2 control loop to maintain regulation. This results in changes in regulator switching frequency, duty cycle, and output ripple in response to changes in load and line. Output voltage ripple will be determined by inductor ripple current working into the ESR of the output capacitors (see Figures 7 and 8).



Trace 1− Regulator Output Voltage (10 mV/div.)
Trace 2− Inductor Switching Node (5.0 V/div.)

Figure 7. Peak−to−Peak Ripple on V_{OUT} = 2.8 V, I_{OUT} = 0.5 A (Light Load)



Trace 1– Regulator Output Voltage (10 mV/div.)
Trace 2– Inductor Switching Node (5.0 V/div.)

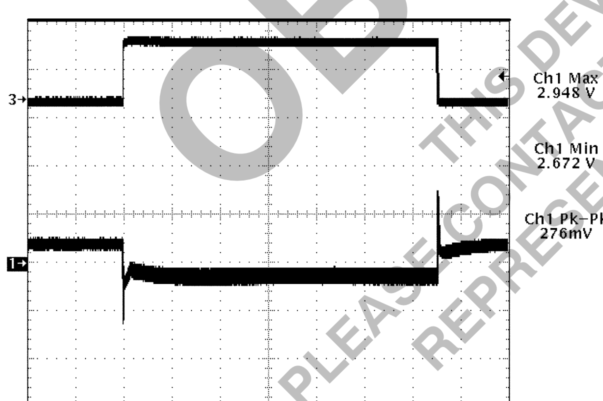
Figure 8. Peak−to−Peak Ripple on V_{OUT} = 2.8 V, I_{OUT} = 13 A (Heavy Load)

Transient Response

The CS5159 V^2 control loop's 100 ns reaction time provides unprecedented transient response to changes in input voltage or output current. Pulse by pulse adjustment of duty cycle is provided to quickly ramp the inductor current to the required level. Since the inductor current cannot be changed instantaneously, regulation is maintained by the output capacitor(s) during the time required to slew the inductor current.

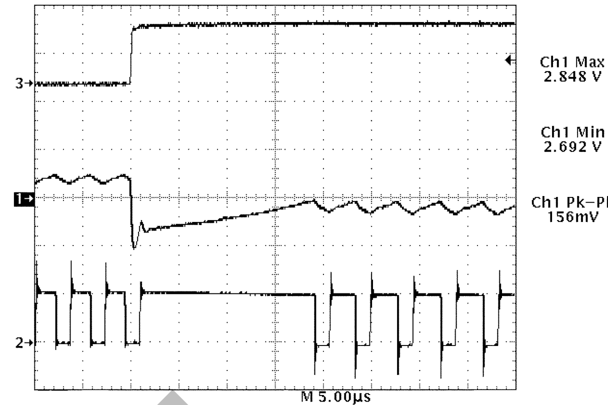
For best transient response, a combination of a number of high frequency and bulk output capacitors are usually used.

If the maximum on time is exceeded while responding to a sudden increase in load current, a normal off time occurs to prevent saturation of the output inductor.



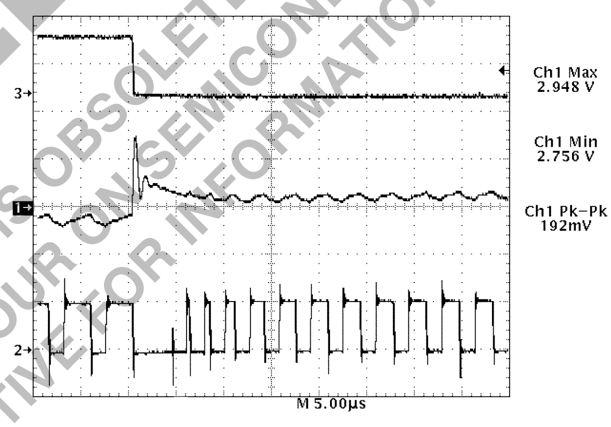
Trace 1– Regulator Output Voltage (1.0 V/div.)
Trace 2– Regulator Output Voltage (20 V/div.)

Figure 9. CS5159 Demonstration Board Response to a 0.5 to 13 A Load Pulse (Output Set for 2.8 V)



Trace 1– Regulator Output Voltage (100 mV/div.)
Trace 2– Inductor Switching Node (5.0 V/div.)
Trace 3– Output Current (0.5 to 13 Amps) (10 A/div.)

Figure 10. CS5159 Demonstration Board Response to 13 A Load Turn On (Output Set for 2.8 V). Upon Completing a Normal Off Time, The V^2 Control Loop Immediately Connects the Inductor to the Input Voltage, Providing 100% Duty Cycle. Regulation is Achieved in Less Than 20 μs



Trace 1– Regulator Output Voltage (100 mV/div.)
Trace 2– Inductor Switching Node (5.0 V/div.)
Trace 3– Output Current (13 to 0,5 Amps) (10 A/div.)

Figure 11. CS5159 Demonstration Board Response to 13 A Load Turn Off (Output Set for 2.8 V). V^2 Control Topology Immediately Connects Inductor to Ground, Providing 0% Duty Cycle. Regulation is Achieved in Less Than 10 μs

PROTECTION AND MONITORING FEATURES

V_{CC1} Monitor

To maintain predictable startup and shutdown characteristics an internal V_{CC1} monitor circuit is used to prevent the part from operating below 3.75 V minimum startup. The V_{CC1} monitor comparator provides hysteresis and guarantees a 3.70 V minimum shutdown threshold.

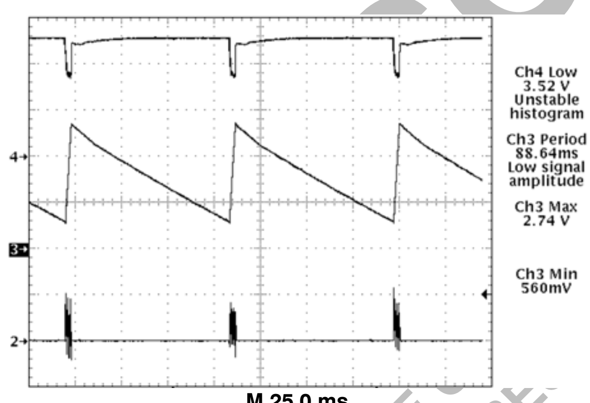
Short Circuit Protection

A lossless hiccup mode short circuit protection feature is provided, requiring only the Soft Start capacitor to implement. If a short circuit condition occurs (V_{FFB} < 1.0 V), the V_{FFB} low comparator sets the FAULT latch. This causes the MOSFET to shut off, disconnecting the regulator from it's input voltage. The Soft Start capacitor is then slowly discharged by a 2.0 μA current source until it reaches it's lower 0.7 V threshold. The regulator will then attempt to restart normally, operating in it's extended off time mode with a 50% duty cycle, while the Soft Start capacitor is charged with a 60 μA charge current.

If the short circuit condition persists, the regulator output will not achieve the 1.0 V low V_{FFB} comparator threshold before the Soft Start capacitor is charged to it's upper 2.5 V threshold. If this happens the cycle will repeat itself until the short is removed. The Soft Start charge/discharge current ratio sets the duty cycle for the pulses (2.0 μA/60 μA = 3.3%), while actual duty cycle is half that due to the extended off time mode (1.65%).

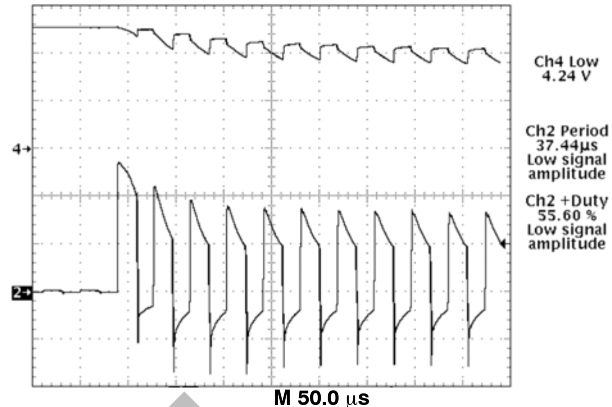
This protection feature results in less stress to the regulator components, input power supply, and PC board traces than occurs with constant current limit protection (see Figures 12 and 13).

If the short circuit condition is removed, output voltage will rise above the 1.0 V level, preventing the FAULT latch from being set, allowing normal operation to resume.



Trace 4− 5.0 V Supply Voltage (2.0 V/div.)
Trace 3− Soft Start Timing Capacitor (1.0 V/div.)
Trace 2− Inductor Switching Node (2.0 V/div.)

Figure 12. CS5159 Demonstration Board Hiccup Mode Short Circuit Protection. Gate Pulses are Delivered While the Soft Start Capacitor Charges, and Cease During Discharge

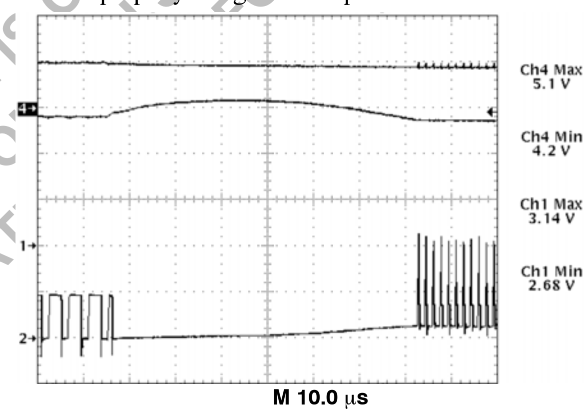


Trace 4− 5.0 V from PC Power Supply (2.0 V/div.)
Trace 2− Inductor Switching Node (2.0 V/div.)

Figure 13. Startup with Regulator Output Shorted

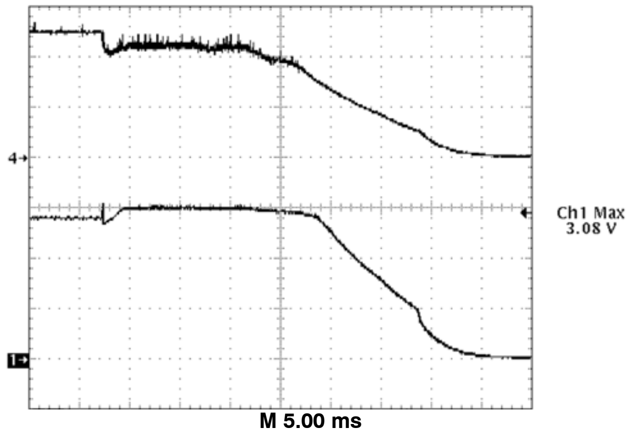
Overvoltage Protection

Overvoltage protection (OVP) is provided as result of the normal operation of the V^2 control topology and requires no additional external components. The control loop responds to an overvoltage condition within 100 ns, causing the top MOSFET to shut off, disconnecting the regulator from it's input voltage. The bottom MOSFET is then activated, resulting in a "crowbar" action to clamp the output voltage and prevent damage to the load (see Figures 14 and 15). The regulator will remain in this state until the overvoltage condition ceases or the input voltage is pulled low. The bottom FET and board trace must be properly designed to implement the OVP function.



Trace 4− 5.0 V from PC Power Supply (5.0 V/div.)
Trace 1− Regulator Output Voltage (1.0 V/div.)
Trace 2− Inductor Switching Node 5.0 V/div.)

Figure 14. OVP Response to an Input−to−Output Short Circuit by Immediately Providing 0% Duty Cycle, Crow−Barring the Input Voltage to Ground



Trace 4− 5.0 V from PC Power Supply (2.0 V/div.)
Trace 1− Regulator Output Voltage (1.0 V/div.)

Figure 15. OVP Response to an Input−to−Output Short Circuit by Pulling the Input Voltage to Ground

External Output Enable Circuit

On/off control of the regulator can be implemented through the addition of two additional discrete components (see Figure 16). This circuit operates by pulling the Soft Start pin high, and the V_{FFB} pin low, emulating a short circuit condition.

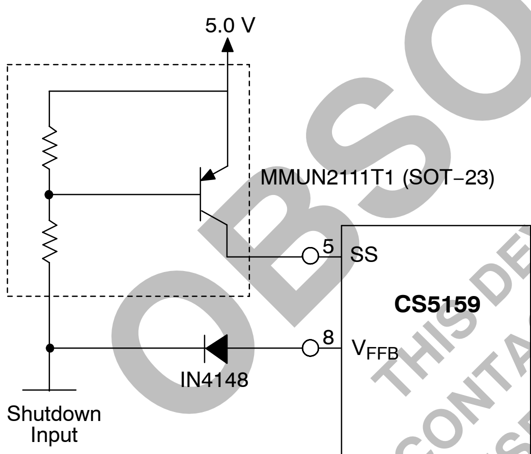


Figure 16. Implementing Shutdown with the CS5159

External Power Good Circuit

An optional Power Good signal can be generated through the use of four additional external components (see Figure 17). The threshold voltage of the Power Good signal can be adjusted per the following equation:

$$V_{Power\ Good} = \frac{(R1 + R2) \times 0.65\ V}{R2}$$

This circuit provides an open collector output that drives the Power Good output to ground for regulator voltages less than $V_{Power\ Good}$.

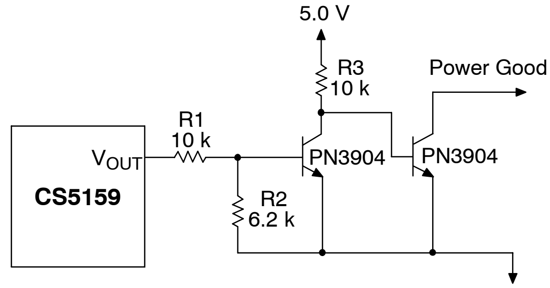
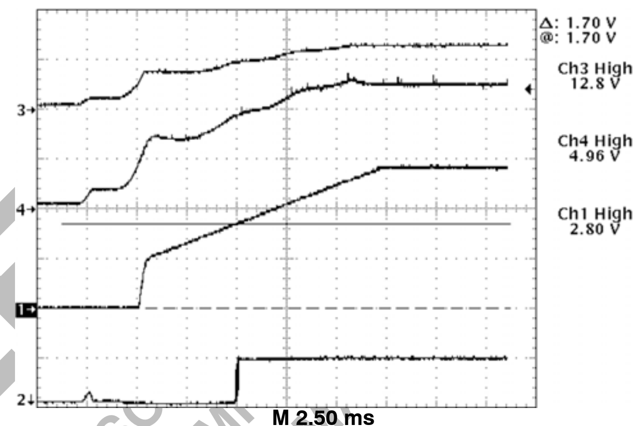


Figure 17. Implementing Power Good with the CS5159



Trace 3 − 12 V Input (V_{CC1}) and (V_{CC2}) (10 V/div.)
Trace 4− 5.0 V Input (2.0 V/div.)
Trace 1− Regulator Output Voltage (1.0 V/div.)
Trace 2− Power Good Signal (2.0 V/div.)

Figure 18. CS5159 Demonstration Board During Power Up. Power Good Signal is Activated when Output Voltage Reaches 1.70 V.

Selecting External Components

The CS5159 can be used with a wide range of external power components to optimize the cost and performance of a particular design. The following information can be used as general guidelines to assist in their selection.

NFET Power Transistors

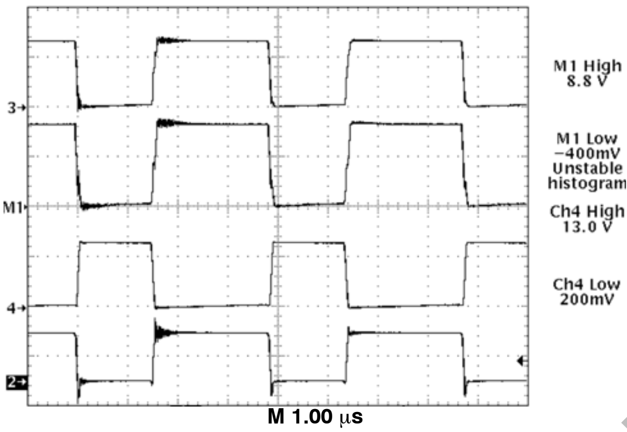
Both logic level and standard MOSFETs can be used. The reference designs derive gate drive from the 12 V supply which is generally available in most computer systems and utilize logic level MOSFETs. Multiple MOSFETs may be paralleled to reduce losses and improve efficiency and thermal management.

Voltage applied to the MOSFET gates depends on the application circuit used. Both upper and lower gate driver outputs are specified to drive to within 1.5 V of ground when in the low state and to within 2.0 V of their respective bias supplies when in the high state. In practice, the MOSFET gates will be driven rail to rail due to overshoot caused by the capacitive load they present to the controller IC. For the

typical application where $V_{CC1} = V_{CC2} = 12$ V and 5.0 V is used as the source for the regulator output current, the following gate drive is provided;

$$V_{GATE(H)} = 12\text{ V} - 5.0\text{ V} = 7.0\text{ V},\ V_{GATE(L)} = 12\text{ V}$$

(see Figure 19.)



Trace 3 = $V_{GATE(H)}$ (10 V/div.)
Math 1 = $V_{GATE(H)}$ − 5.0 V_{IN}
Trace 4 = $V_{GATE(L)}$ (10 V/div.)
Trace 2− Inductor Switching Nodes (5.0 V/div.)

Figure 19. CS5159 Gate Drive Waveforms Depicting Rail to Rail Swing

The most important aspect of MOSFET performance is RDS_{ON}, which effects regulator efficiency and MOSFET thermal management requirements.

The power dissipated by the MOSFETs may be estimated as follows;

Switching MOSFET:

$$\text{Power} = I_{LOAD}{}^2 \times RDS_{ON} \times \text{duty cycle}$$

Synchronous MOSFET:

$$\text{Power} = I_{LOAD}{}^2 \times RDS_{ON} \times (1 - \text{duty cycle})$$

Duty Cycle =

$$\frac{V_{OUT} + (I_{LOAD} \times RDS_{ON\ OF\ SYNCH\ FET})}{\left[\begin{array}{l} V_{IN} + (I_{LOAD} \times RDS_{ON\ OF\ SYNCH\ FET}) \\ - (I_{LOAD} \times RDS_{ON\ OF\ SWITCH\ FET}) \end{array}\right]}$$

Off Time Capacitor (C_{OFF})

The C_{OFF} timing capacitor sets the regulator off time:

$$T_{OFF} = C_{OFF} \times 4848.5$$

When the V_{FFB} pin is less than 1.0 V, the current charging the C_{OFF} capacitor is reduced. The extended off time can be calculated as follows:

$$T_{OFF} = C_{OFF} \times 24,242.5$$

Off time will be determined by either the T_{OFF} time, or the time out timer, whichever is longer.

The preceding equations for duty cycle can also be used to calculate the regulator switching frequency and select the C_{OFF} timing capacitor:

$$C_{OFF} = \frac{\text{Perioid} \times (1 - \text{duty cycle})}{4848.5}$$

where:

$$\text{Period} = \frac{1}{\text{switching frequency}}$$

Schottky Diode for Synchronous MOSFET

A Schottky diode may be placed in parallel with the synchronous MOSFET to conduct the inductor current upon turn off of the switching MOSFET to improve efficiency. The CS5159 reference circuit does not use this device due to it's excellent design. Instead, the body diode of the synchronous MOSFET is utilized to reduce cost and conducts the inductor current. For a design operating at 200 kHz or so, the low non−overlap time combined with Schottky forward recovery time may make the benefits of this device not worth the additional expense (see Figure 8, channel 2). The power dissipation in the synchronous MOSFET due to body diode conduction can be estimated by the following equation:

$$\text{Power} = V_{BD} \times I_{LOAD} \times \text{conduction time} \times \text{switching frequency}$$

Where V_{BD} = the forward drop of the MOSFET body diode. For the CS5159 demonstration board as shown in Figure 8;

$$\text{Power} = 1.6\text{ V} \times 13\text{ A} \times 100\text{ ns} \times 233\text{ kHz} = 0.48\text{ W}$$

This is only 1.3% of the 36.4 W being delivered to the load.

Input and Output Capacitors

These components must be selected and placed carefully to yield optimal results. Capacitors should be chosen to provide acceptable ripple on the input supply lines and regulator output voltage. Key specifications for input capacitors are their ripple rating, while ESR is important for output capacitors. For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.

Output Inductor

The inductor should be selected based on its inductance, current capability, and DC resistance. Increasing the inductor value will decrease output voltage ripple, but degrade transient response.

THERMAL MANAGEMENT

Thermal Considerations for Power MOSFETs and Diodes

In order to maintain good reliability, the junction temperature of the semiconductor components should be kept to a maximum of 150°C or lower. The thermal impedance (junction to ambient) required to meet this requirement can be calculated as follows:

$$\text{Thermal Impedance} = \frac{T_{JUNCTION(MAX)} - T_{AMBIENT}}{\text{Power}}$$

A heatsink may be added to TO−220 components to reduce their thermal impedance. A number of PC board layout techniques such as thermal vias and additional copper foil area can be used to improve the power handling capability of surface mount components.

EMI Management

As a consequence of large currents being turned on and off at high frequency, switching regulators generate noise as a consequence of their normal operation. When designing for compliance with EMI/EMC regulations, additional components may be added to reduce noise emissions. These components are not required for regulator operation and experimental results may allow them to be eliminated. The input filter inductor may not be required because bulk filter and bypass capacitors, as well as other loads located on the board will tend to reduce regulator di/dt effects on the circuit board and input power supply. Placement of the power component to minimize routing distance will also help to reduce emissions.

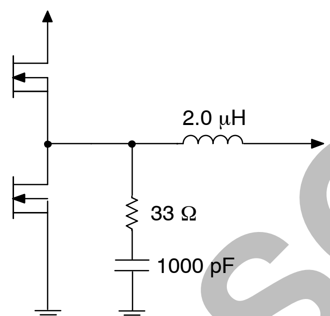


Figure 20. Filter Components

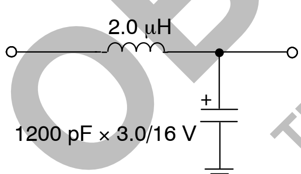


Figure 21. Input Filter

Layout Guidelines

1. Place 12 V filter capacitor next to the IC and connect capacitor ground to pin 11 (PGND).
2. Connect pin 11 (PGND) with a separate trace to the ground terminals of the 5.0 V input capacitors.
3. Place fast feedback filter capacitor next to pin 8 (V_{FFB}) and connect it's ground terminal with a separate, wide trace directly to pin 14 (LGND).
4. Connect the ground terminals of the Compensation capacitor directly to the ground of the fast feedback filter capacitor to prevent common mode noise from effecting the PWM comparator.
5. Place the output filter capacitor(s) as close to the load as possible and connect the ground terminal to pin 14 (LGND).
6. Connect the V_{FB} pin directly to the load with a separate trace (remote sense).
7. Place 5.0 V input capacitors close to the switching MOSFET and synchronous MOSFET.

Route gate drive signals $V_{GATE(H)}$ (pin 10) and $V_{GATE(L)}$ (pin 12 when used) with traces that are a minimum of 0.025 inches wide.

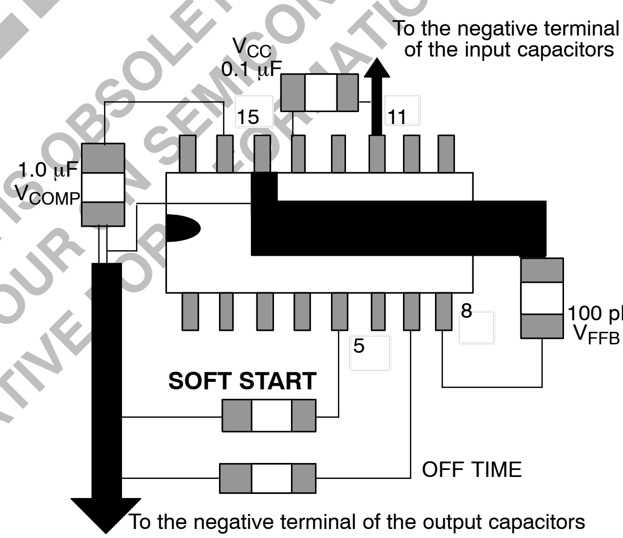


Figure 22. Layout Guidelines

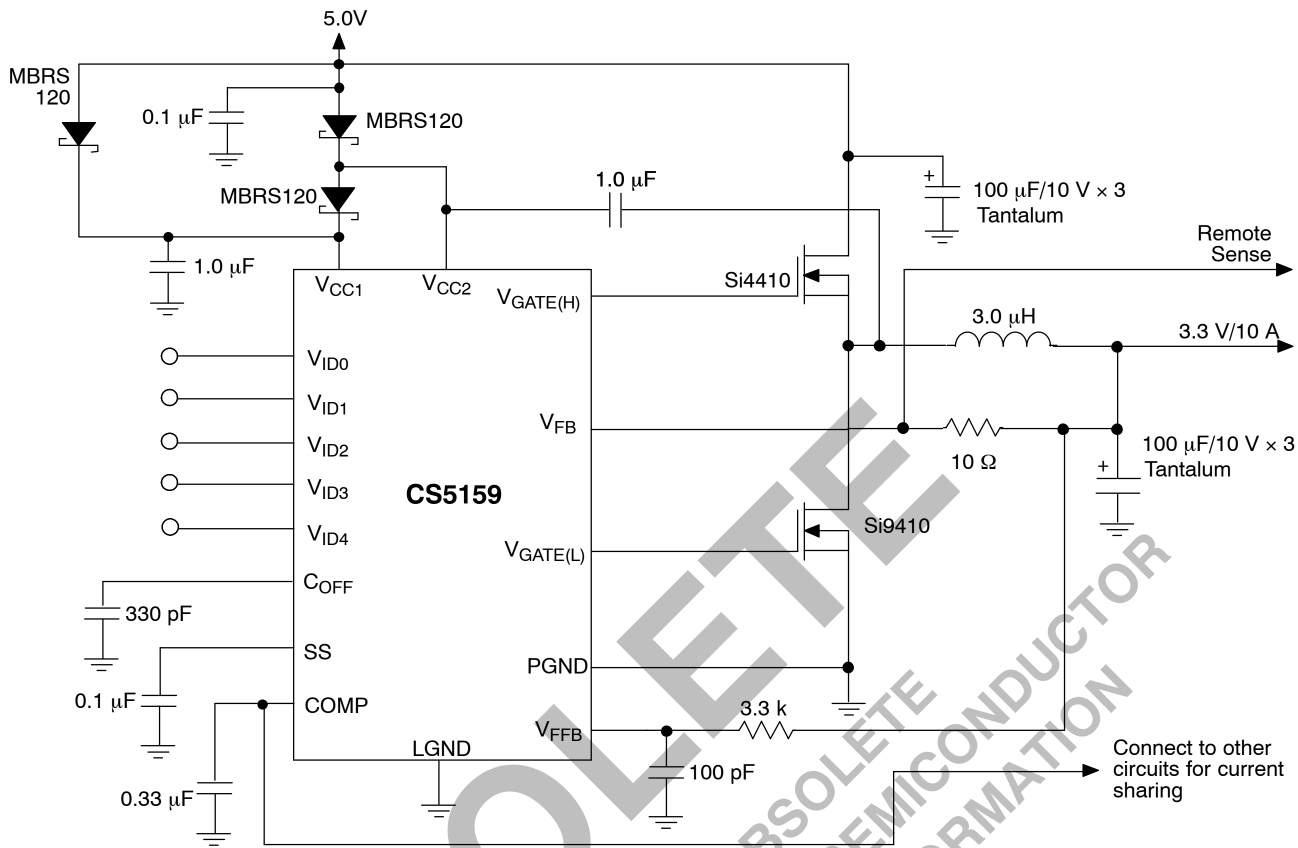


Figure 23. Additional Application Diagram, 5.0 V to 3.3 V/10 A Converter with Current Sharing

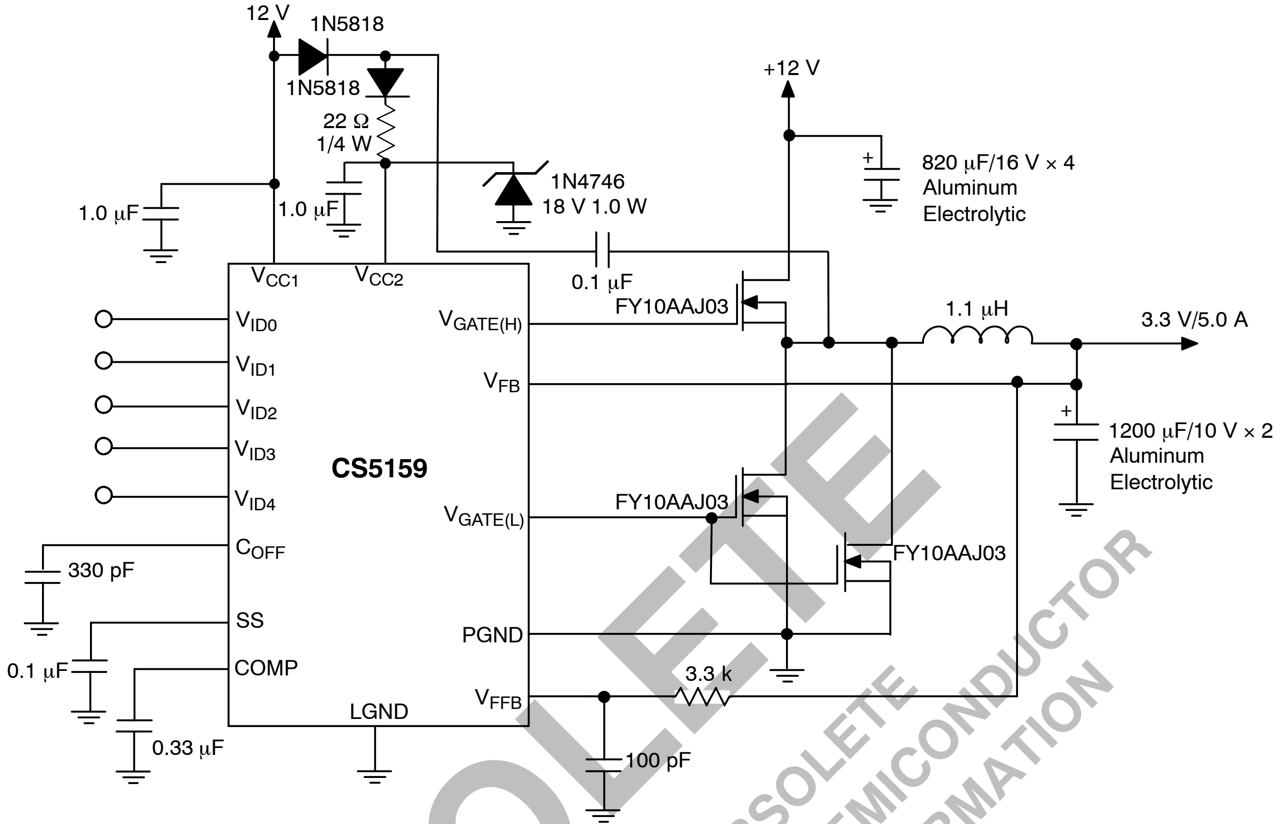


Figure 24. Additional Application Diagram, 12 V to 3.3 V/5.0 A Converter With Remote Sense

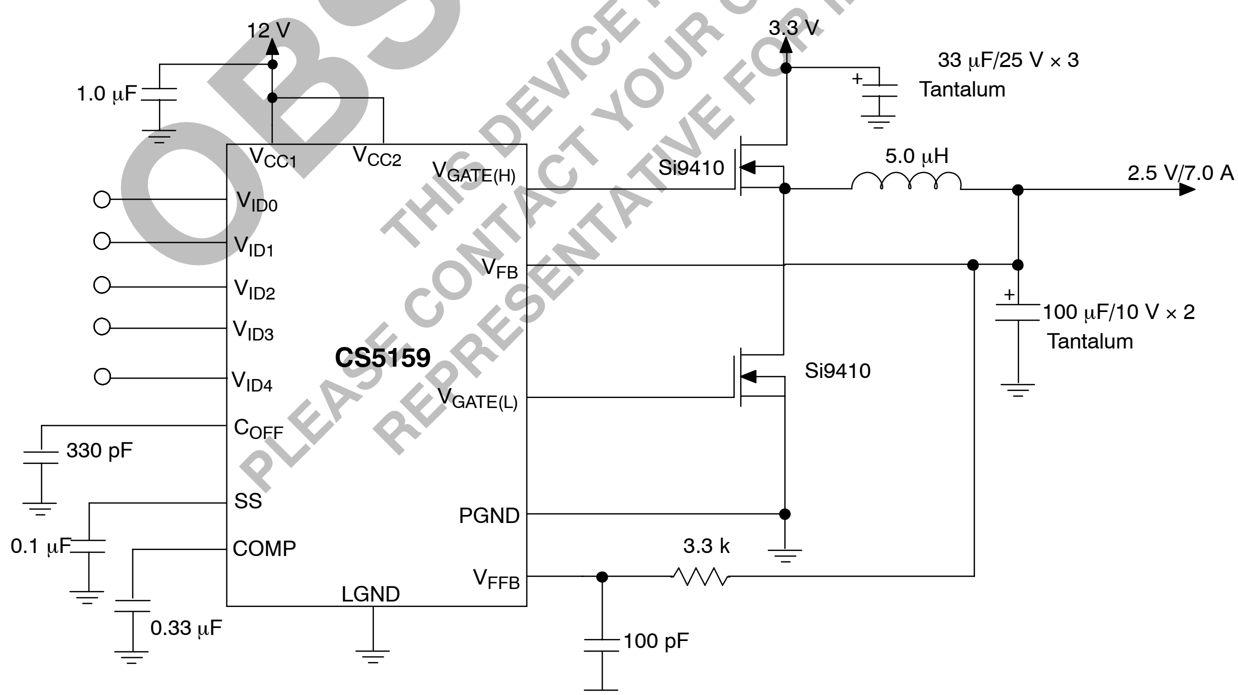
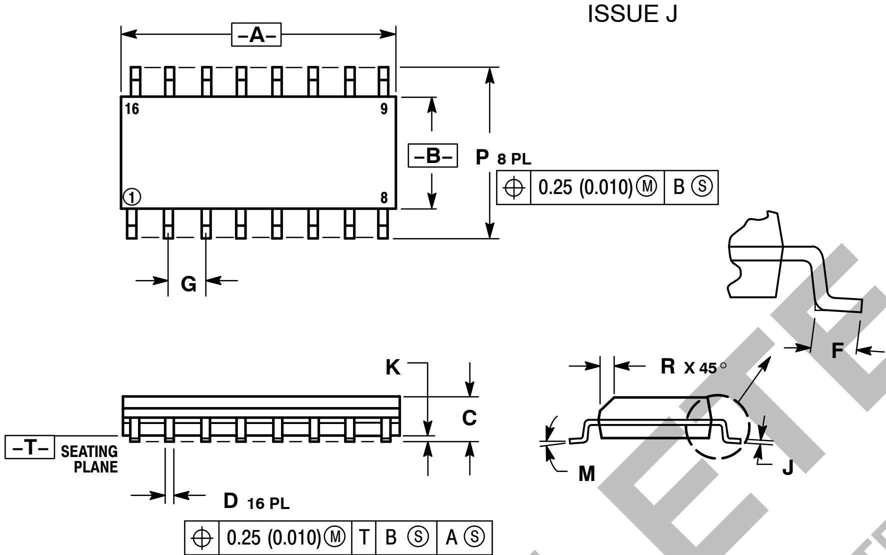


Figure 25. Additional Application Diagram, 3.3 V to 2.5 V/7.0 A Converter with 12 V Bias

PACKAGE DIMENSIONS

SO−16
D SUFFIX
CASE 751B−05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

PACKAGE THERMAL DATA

Parameter		16−SO	Unit
$R_{\Theta JC}$	Typical	28	°C/W
$R_{\Theta JA}$	Typical	115	°C/W

V^2 is a trademark of Switch Power, Inc.
Pentium is a registered trademark of Intel Corporation.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative